CLAIMS

1. (Cancelled)

2. (previously amended) A transparent port for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol, wherein said PLT translates said user signal into a data signal whenever said rate R1 corresponds to a provisioned first protocol and passes said user signal unchanged whenever said rate R1 is not recognized by said processing unit.

3. (Currently amended) A transparent port as claimed in claim 2 ~~1~~, wherein said PLT performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

4. (original) A transparent port as claimed in claim 2, further comprising a mapping unit for rearranging the bits of said data signal into a container signal of a rate R corresponding to a second protocol.

5. (Currently amended) A transparent port as claimed in claim 2 ~~1~~, wherein said PLT comprises logic gates configured to perform measurement of a provisioned parameter.

6. (Currently amended) A transparent port as claimed in claim 2 ~~1~~, wherein said PLT is a programmable gate array.

7. (previously amended) A transparent port for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol wherein said set of performance parameters includes a previous section fail indicator.

8. (currently amended) A transparent port as claimed in claim 7 ~~1~~, wherein said set of performance parameters includes one or more of signal strength, clock continuity and jitter.

9. (currently amended) A transparent port as claimed in claim 7 ~~1~~, wherein said PLT performs one ore more of a framing, an error count, a code conversion, and a parity correction operation.

10. (Previously Amended) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol;

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; and

a reverse mapping unit for rearranging the bits of a container signal of a second protocol into said data signal of said first protocol.

11. (original) A transparent port as claimed in claim 10, wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

12. (Cancelled).

13. (original) A transparent port as claimed in claim 10, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

14. (original) A transparent port as claimed in claim 10, wherein said PLI is a programmable gate array.

15. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes a previous section fail indicator.

16. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

17. (original) A transparent port as claimed in claim 10, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

18. (original) A method for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network as a transparent tributary, comprising:

at a transmit terminal, selecting a container signal of a rate R, higher than said rate R1;

detecting the rate R1 of said continuous digital signal and determining a first protocol corresponding to said rate R1;

measuring according to a first protocol a set of performance parameters on said continuous signal and reporting said set of performance parameters; and

translating said set of performance parameters from said first protocol to a second protocol characterizing said container signal and providing said translated set into said container signal.

19. (original) A method as claimed in claim 18, further comprising transmitting said container signal from said transmit terminal to a receive terminal.

20. (original) A method as claimed in claim 18, further comprising informing said receive terminal of said rate R1 and of said first protocol through signaling.

21. (original) A method as claimed in claim 20, further comprising:

at the receive terminal, recovering said container signal;

extracting said set of performance parameters from said container signal; and

reconstituting said continuous signal based on said rate R1.

22. (original) A method as claimed in claim 21, further comprising transmitting said continuous signal with said set of performance parameter to a user.

23. (Previously presented) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol;

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

24. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

25. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI is a programmable gate array.

26. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.

27. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

28. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

29. (Previously presented) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1', wherein said set of performance parameters includes a previous section fail indicator;

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol; and

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal.

30. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

31. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI is a programmable gate array.

32. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

33. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.